WHAT IS CLAIMED IS :

(a) 1. A data transmitter for receiving a single-ended binary input signal and converting the single-ended binary signal to a differential binary output signal, the data transmitter comprising:a first and a second conduction paths connected in parallel between a first and a second nodes;

(b) a first and a second switches connected in series in the first conduction path, wherein the first switch is located near the first node, and the second swicth is located near the second node;

(c) a third and a forth switches connected in series in the second conduction path, wherein the third switch is located near the first node, and the fourth switch is located near the second node;

(d) NMOS transistor used as a source follower having a drain connected to voltage source, a gate connected to a first driving voltage, and a source connected to the first node, for providing current to the first and the second conduction paths via the first node; and

(e) PMOS transistor used as a source follower having a drain connected to the ground, a gate connected to a second driving voltage, a source connected to the second node for receiving current from the first and the second conduction paths via the second node;

wherein the press-control terminals of the first switch, the second switch, the third switch and the fourth switch are respectively provided with the single-ended binary input signal or the reverse direction signal thereof for cutting off the second and the third switches when the first and the fourth switches are turned on, and for cutting off the first and the fourth switches when the second and the third switches are turned on; the differential binary output signal is pulled out by a pair of output terminals, one of the output terminal is connected to the connection area of the first and the second switches within the first conduction path, while the other output terminal is connected to the connection area of the third and the fourth switches within the second conduction path.

2. A data transmitter as set forth in Claim 1, wherein the first and the third switches are PMOS switches, and the second and the fourth switches are NMOS switches,

and the first driving voltage is generated by the first driving voltage output circuit, and the second driving voltage is generated by the second driving voltage output circuit, wherein the first driving voltage output circuit comprising:

(a) a first fixed current source having a bottom terminal connected to the ground;

(b) a first NMOS transistor and a first PMOS transistor, wherein the sources of both the transistor are connected, the drain of the first NMOS transistor is connected to the voltage source, the gate is connected to the gate of NMOS that is used as the source follower, the drain of the first PMOS transistor is connected to the top terminal of the first fixed current source, and the gate is connected to the ground; and

(c) a first comparator having a positive input terminal connected to a first reference voltage, a negative input terminal connected to the top terminal of the first fixed current source, and the output terminal being connected to the gate of the first NMOS transistor; and

the second driving voltage output circuit comprising:

(d) a second fixed current source having a top terminal connected to the ground;

(e) a second NMOS transistor and a second PMOS transistor, wherein the sources of both the transistors are connected, andthe drain of the second PMOS is connected to the ground; the gate is connected to the gate of PMOS transistor that is used as the source follower; the drain of the second NMOS transistor is connected to the bottom terminal of the second fixed current source, and the gate is connected to voltage source; and

(f) a second comparator having a positive input terminal for receiving a second reference voltage, and a negative input terminal connected to the

bottom terminal of the second fixed current source, andan output terminal connected to the gate of the second PMOS transistor.

3. A data transmitter as set forth in Claim 1, wherein the first and the third switches are PMOS switches, and the second and the fourth switches are NMOS switches, and the first driving voltage is generated by the first driving voltage output circuit, and the second driving voltage is generated by the second driving voltage output circuit, wherein the first driving voltage output circuit further comprises:

(a) a first fixed current source having a top terminal connected to a voltage source;

(b) a first resistor having a first terminal connected to the ground; and

(c) a first NMOS transistor and a first PMOS transistor, wherein the source of both the transistors are connected, the drain of the first NMOS transistor is connected to the gate, and the drain is connected in parallel at the bottom terminal of the first fixed current source, the gate is connected to the gate of NMOS transistor that is used as the source follower, the drain of the first PMOS transistor is connected to the second terminal of the resistor, and the gate is connected to the ground;

the second driving voltage output circuit further comprises:

(d) a second fixed current source having a bottom terminal connected to the ground;

(e) a second resistor having a first terminal connected to voltage source; and

(f) a second NMOS transistor and a second PMOS transistor, wherein the sources of both the transistors are connected, the drain of the second PMOS is connected to the gate, and the drain is connected in parallel at the top terminal of the second fixed current source, the gate is connected

to the gate of PMOS transistor that is used as the source follower, the drain of the second PMOS transistor is connected to the second terminal of the resistor, and the gate is connected to the voltage source.

4. A data transmitter for receiving a single-ended binary input signal and converting the single-ended binary signal to a differential binary output signal, the data transmitter comprising:

(a) a first and a second conduction paths connected in parallel between a first and a second nodes;

(b) a first and a second switches connected in series in the first conduction path, wherein the first switch is located near the first node, and the second switch is located near the second node.

(c) a third and a forth switches connected in series in the second conduction path, wherein the third switch is located near the first node, and the fourth switch is located near the second node;

(d) npn transistor that is used as an emitter follower having a collector connected to voltage source, a base connected to a first driving voltage, an emitter connected to the first node for providing current to the first and the second conduction paths via the first node; and

(e) pnp transistor that is used as an emitter follower having a collector connected to the ground, a base connected to the second driving voltage, an emitter connected to a second node for receiving current from the first and the second conduction paths via the second node;

wherein the press-control terminals of the first switch, the second switch, the third switch and the fourth switch are respectively provided with the single-ended binary input signal or the reverse direction signal thereof for cutting off the second and the third switches when the first and the fourth switches are turned on, and for cutting off the first and the fourth switches when the second and the third switches are turned on; the differential binary output signal is pulled out by a pair of output terminals, wherein one of the output terminal is connected to the connection area of the first and the second

switches within the first conduction path, and the other output terminal is connected to the connection area of the third and the fourth switches within the second conduction path.

5. A data transmitter as set forth in Claim 4, wherein the first and the third switches are pnp switches, and the second and the fourth switches are npn switches, and the first driving voltage is generated by the first driving voltage output circuit, and the second driving voltage is generated by the second driving voltage output circuit, wherein the first driving voltage output circuit comprises:

(a) a first fixed current source having a bottom terminal connected to the ground;

(b) a first npn transistor and a first pnp transistor, wherein the emitters of both the transistor are connected, the collector of the first npn transistor is connected to voltage source, the base is connected to the base of npn that is used as the emitter follower, the collector of the first pnp transistor is connected to the top terminal of the first fixed current source, and the base is connected to the ground; and

(c) a first comparator having a positive input terminal connected to a first reference voltage, a negative input terminal connected to the top terminal of the first fixed current source, and an output terminal connected to the base of the first npn transistor; and

the second driving voltage output circuit comprises

(d) a second fixed current source having a top terminal connected to the ground;

(e) a second npn transistor and a second pnp transistor, wherein the emitters of both the transistors are connected, the collector of the second pnp is connected to the ground, and the base is connected to the base of pnp transistor that is used as the emitter follower, the collector of the second

npn transistor is connected to the bottom terminal of the second fixed current source, and the base is connected to voltage source; and

(f) a second comparator having a positive input terminal for receiving a second reference voltage, a negative input terminal connected to the bottom terminal of the second fixed current source, and an output terminal connected to the base of the second pnp transistor.

6. A data transmitter as set forth in Claim 4, wherein the first and the third switches are pnp switches, and the second and the fourth switches are npn switches, and the first driving voltage is generated by the first driving voltage output circuit, and the second driving voltage is generated by the second driving voltage output circuit, wherein the first driving voltage output circuit comprises:

(a) a first fixed current source having a top terminal connected to a voltage source;

(b) a first resistor having a first terminal connected to the ground; and

(c) a first npn transistor and a first pnp transistor, wherein the emitters of both the transistors are connected, the collector of the first npn transistor is connected to the base, and the collector is connected in parallel at the bottom terminal of the first fixed current source, the base is connected to the base of npn transistor that is used as the emitter follower, the collector of the first pnp transistor is connected to the second terminal of the resistor and the base is connected to the ground; and

the second driving voltage output circuit comprises

(d) a second fixed current source having a bottom terminal connected to the ground;

(e) a second resistor having a first terminal connected to voltage source; and

(f) a second npn transistor and a second pnp transistor, wherein the emitters of both the transistor are connected, the collector of the second pnp is connected to the base, and the collector is connected in parallel at the top terminal of the second fixed current source, the base is connected to the base of npn transistor that is used as the emitter follower, the collector of the second npn transistor is connected to the second terminal of the resistor, and the base is connected to voltage source.